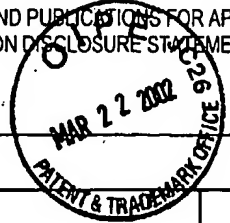


FORM PTO-1449(Modified) LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT	ATTY. DOCKET NO.: A00312.70418/SJH/MXS	SERIAL NO.: 10/039,867
	APPLICANT: Jieming Qi	
	FILING DATE: December 20, 2001	GROUP: 2121

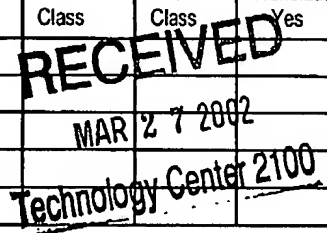


U.S. PATENT DOCUMENTS

Exam Init	Ref Des	Document No.	Date	Name	Class	Sub Class	FILING DATE If Appropriate

FOREIGN PATENT DOCUMENTS

		Country & Doc. No. (11)	Pub. Date (43)		Class	Sub Class	Translation Yes No



OTHER ART

(Including Author, Title, Date, Pertinent Pages, Publication, Etc.)

Man J V			Abut-Khater et al., "Circuit Techniques for CMOS Low-Power High Performance Multipliers", IEEE Journal of Solid-State Circuits, Vol. 31, No. 10, October 1996, pp. 1535-1546;
			Goto et al., "A 4.1-ns Compact 54 X 54-b Multiplier Utilizing Sign-Select Booth Encoders", IEEE Journal of Solid-State Circuits, Vol. 32, No. 11 November 1997; pp. 1676-1681;
			Ohkubo et al., "A 4.4 ns CMOS 54 x 54-b Multiplier Using Pass-Transistor Multiplexer", IEEE Journal of Solid-State Circuits, Vol. 30, No. 3, March 1995, pp. 251-257;
			Yeh et al, "High-Speed Booth Encoded Parallel Multiplier Design" IEEE Transactions on Computers, Vol. 49, No. 7, July 2000, pp. 692-710

EXAMINER 	DATE CONSIDERED
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EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered.